an unsegmented via located through the first and second etch stop layers and interlevel dielectric layers, the via extending to and contacting the first metal feature, the via being void of a landing pad between the first and second interlevel dielectric layers;

a second metal feature located adjacent the unsegmented via and extending through the second interlevel dielectric layer and the second etch stop layer and terminating at the first interlevel dielectric layer; and

a dual damascene structure adjacent the second metal feature and having a damascene trench portion extending through the second interlevel dielectric layer and the second etch stop layer and terminating at the first interlevel dielectric layer and further including a damascene via portion extending through the first interlevel dielectric layer and the first etch stop layer and connecting the trench portion to the first metal feature.

(2) Please cancel Claims 22, 23 and 26 without prejudice or disclaimer.

(3) Please amend Claim 28 as follows:

28. (Amended) The semiconductor device as recited in Claim 27 further including a second via that extends through the third dielectric layer and contacts the landing pad.

REMARKS

The Applicant originally submitted Claims 1-28 in the present application. Pursuant to a restriction requirement, Claims 1-20 were previously withdrawn without traverse. The Applicant